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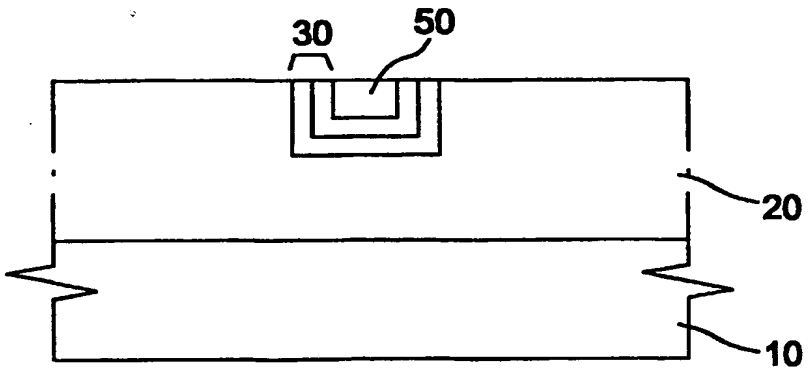
(54) Title: METHOD OF FABRICATING SEMICONDUCTOR DEVICE EMPLOYING COPPER INTERCONNECT STRUCTURE



(57) Abstract: The present invention provides a method of forming interconnect structure in a process for fabricating semiconductor device, which enables high-reliability copper interconnect. The present invention uses the structure comprised of TiN layer (32) and intermediate aluminum layer (34) as a diffusion barrier. A copper layer (40) is deposited on the aluminum layer (34), after aluminum layer (34) is deposited on the TiN layer (32). At this time, with the aluminum layer (34) being made to the minimum thickness, metallization is formed substantially with the copper.

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METHOD OF FABRICATING SEMICONDUCTOR DEVICE EMPLOYING COPPER INTERCONNECT STRUCTURE

Technical Field

The present invention relates to a method of fabricating a semiconductor device, and more particularly, to a method of forming an interconnect structure in a process for fabricating a semiconductor device. This application is based on Korean patent application No. 99-020828, which is incorporated by reference herein for all purposes.

Background Art

There are roughly two kinds of processes in fabricating a semiconductor integrated device. One is related to a process for forming components on a silicon substrate, and the other to a process for interconnecting the components electrically. The process for interconnecting the components electrically is called "metallization", which is important in improving yield and reliability as the integrity of the device continues to increase .

Aluminum has been widely used for metallization material. However, as the integrity of the device increases, the width of the metallization decreases and the total length of the metallization increases. Therefore, the delay time of a signal transfer represented as resistance-capacitance (RC) time constant increases. Also, as the width of the metallization decreases, short of metal interconnects due to electromigration and stress migration becomes a serious problem. Thus, to make a semiconductor device which has faster operation speed and higher reliability, the process for metallization has been changed to use copper having lower resistivity

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and higher resistance to electromigration and stress migration than those of aluminum.

Though copper has low resistivity and high melting point, it has not other physical property which aluminum has. For example, copper has not dense protection surface film such as Al_2O_3, and does not adhere well to silicon dioxide. Also, it is difficult to perform dry etching process to copper. It is well-known that diffusion coefficient of copper in silicon is about 10^6 times as large as that of aluminum, and copper diffused into silicon has deep energy level between its band gaps. In addition, it is also well-known that diffusion coefficient of copper in silicon dioxide is large, which makes worse the insulating property between the copper interconnections. The large diffusion coefficient of copper in silicon and silicon dioxide deteriorates the reliability of a semiconductor device. Therefore, it is essential to develop a diffusion barrier which can prevent the diffusion of copper into silicon and silicon dioxide. However, it takes much time to develop high-reliable diffusion barrier for copper, which may cause to delay common use of a semiconductor device employing copper metallization structure.

Disclosure of the Invention

The object of the present invention is to provide a method of forming interconnect structure in a process for fabricating a semiconductor device, which enables high-reliabilty copper interconnect.

The present invention uses the structure comprised of TiN layer and an intermediate aluminum layer as a diffusion barrier in the copper metallization process, considering that the effectiveness as a diffusion barrier of TiN layer, when used in aluminum metallization. That is, in the present invention, a copper layer is deposited on the aluminum layer, after aluminum layer is deposit d on the TiN layer. Aluminum is then diffused

into the TiN layer so as to stuff the grain boundary of the TiN effectively to prevent the diffusion of copper diffused to the TiN layer afterward. Certain thickness of aluminum remains at the interface in between the copper and TiN and acts as a diffusion barrier by itself. At this time, with the aluminum layer being made to the minimum thickness, metallization is formed substantially with copper. Furthermore, the diffusion between aluminum and copper should be minimized in order that the resistivity of copper is not changed. When the diffusion barrier commonly used in aluminum metallization is coupled with the aluminum layer, the structure of the coupled layer functions as a excellent diffusion layer preventing the diffusion of the copper in copper metallization effectively. The use of TiN layer is necessary since it acts as a seeding for CVD-Al and as a etch-stop layer for CMP process.

Brief Description of the Drawings

The above objectives and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIGS. 1 to 6 illustrate an embodiment of a method for forming copper interconnect structure according to the present invention;

FIG. 7 is a graph showing the experimental measurement of sheet resistance of four different samples depending on the thickness of extremely thin aluminum layer and annealing temperature.

FIGS. 8A to 8D are photos observed by scanning electron microscopy showing etch pits of silicon surface after etching a copper layer, an aluminum layer and a TiN layer according to an embodiment of the present invention.

Embodiments

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A dIffusion barrier means a material inserted between two materials to prevent any mixture thereof. In a process for fabricating a semiconductor device, the diffusion barrier is used to prevent the diffusion of metallization material into a dielectric film as well as the diffusion between the metallization material and the semiconductor substrate.

The diffusion barriers are roughly classified into a passive barrier, a non-barrier, a single crystal barrier, a sacrificial barrier, and stuffed barrier. If a diffusion barrier is stable thermodynamically between the metallization material and the substrate, it is a passive barrier or a non-barrier. If the barrier is unstable thermodynamically to react to the metallization material and the substrate, it is a sacrificial barrier. Whether the diffusion barrier stable themodynamically becomes a passive barrier or a non-barrier is related to a diffusion through a grain boundary of the diffusion barrier. That is, if the material of the barrier hardly diffuses through the grain boundary , the barrier is a passive barrier, and if not, it is a non-passive barrier. The sacrificial barrier prevents a diffusion of materials by reacting with the metallization material and the substrate. The sacrificial barrier is exhausted out by reacting itself. Therefore, it can serve as the diffusion barrier but does not function as the diffusion barrier, after it is exhausted out completely.

Generally, a thin-filmed layer deposited with a process for fabricating the thin film forms polycrystal. Herein, as a diffusion through a grain boundary in a polycrystalline thin film is easier than a bulk, it is very important to prevent the diffusion through the grain boundary. There are provided two methods to prevent the diffusion through the grain boundary. Firstly, it is to use single crystal which has not a grain boundary or amorphous crystal as a diffusion barrier. Secondly, it is to block the grain boundary by different elements. Blocking the grain boundary in

polycrystalline thin film is referred to "stuffing ", and a barrier for stuffing is referred to "stuffed barrier".

The stuffing methods proposed up to now is divided into methods to use N_2 and O_2. The stuffing method to use N_2 is researched to extract N_2 at the grain boundary, with depositing a material containing N_2 over the limit the thin film can contain. The stuffing method to use O_2 is researched to stuff the thin film by exposing the thin film in the air or annealing the thin film in N_2 ambient so that O_2 diffuses through the grain boundary, after depositing the thin film. However, according to the experimental data of the present invention, the effects of the stuffing with N_2 or O_2 are good to aluminum, but the stuffing with N_2 or O_2 does not effect on the copper.

This is because the most of O_2 contained in titanium nitride (TiN) layer by annealing diffuses along the grain boundary and oxidize the surface of the TiN bulk ,so that the O_2 bonds with titanium to form Al_2O_3 by reacting easily with aluminum diffused along the grain boundary. However, the O_2 bonded with titanium does not react with copper. The reason of such a phenomenon is that aluminum can form aluminum oxide compound by reacting with O_2 bonded with titanium, as the enthalpy of formation of aluminum oxide compound is larger than that of titanium oxide compound , whereas copper can not react with O_2 bonded with titanium, as the enthalpy of formation of copper oxide compound is smaller than that of titanium oxide compound, as shown in Table 1. Table 1 shows the enthalpy of formation in oxide compound of titanium, aluminum and copper.

Table 1: Enthalpy of formation in oxide compound of titanium,aluminum and copper.

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Bonded form	Phase	Enthalpy of formation at a temperature of 298K (kJ/mole)
Tl-O	TiO	-519.7
	Ti_2O_3	-1521.6
	Ti_3O_5	-2457.2
	TiO_2	-944.0
Al-O	Al_2O_3	-1675.7
Cu-O	CuO	-168.6
	Cu_2O	-157.3

As described above, thin- filmed TiN layer functions as an execllent stuffed barrier against aluminum, whereas it functions as the non-barrier for copper which permits fast diffusion against copper. Also, as copper hardly react with N_2 as well as O_2, it is also difficult to improve the efficiency of the TiN layer by adding impurities.

Therefore, the demand for developing new materials as a diffusion barrier suitable for copper metallization arises. For example, Ta or TaN with physical vapor deposition (PVD) method is spotlighted as new materials and it is tried to realize to deposit such materials with PVD.

Meanwhile, as a line-of-sight deposition method such a sputtering method, makes non-uniformly the thicknes of submicron unit-contact hole which has large aspect ratio, it is difficult to apply to ultra-high integrated device. Therefore, a research for forming a diffusion barrier using chemical vapor deposition (CVD) having excellent characteristic for step coverage continues to be carried out.

As TiN has a melting point of about 3220°C to be thermally stable and low resistive, it has been used for a diffusion barrier between aluminum alloy and silicon substrate. CVD methods for the TiN layer roughly

classified into a method using inorganic compounds for source gas, such as titanium tetrachloride ($TiCl_4$) or titanium tetraiodide (TiI_4) and NH_3, and a method using metal-organic compounds for precursor, such as tetrakisdimethylamido titanium (TDMAT) or tetrakisdiethylamido titanium (TDEAT).

Several TiN layers having good characteristics for physical property and step coverage are reported by many researchers, and it is known that such TiN layers can be used successfully for adhesion layers and seeding layer for chemical vapor deposition. However, the reports to characteristics of TiN layers deposited with CVD as a diffusion barrier against copper are few. Also, it is reported that characteristics of such TiN layers are poor.

Meanwhile, as tantalum nitride (TaN) is thermally stable against copper, a research for using the TaN for diffusion layer in copper metallization process has been performed. It is already confirmed that the TaN has an excellent characteristics for the diffusion barrier against copper. Research for the CVD methods of the TaN layer has been performed using inorganic compounds for source gas, such as tantalum pentachloride ($TaCl_5$) or tantalum pentabromide ($TaBr_5$) ,NH3 or N_2, and using organic compounds for precursor, such as pentadimethylamido tantalum (PDMAT), pentadiethylamido tantalum (PDEAT) or tertbutylimidotrisdiethylamido tantalum (TBTDET).

However, in a Ta-N group, as there is Ta_3N_5 thermodynamically more stable than TaN, it is not easy to deposit a TaN layer having good physical property by CVD.

Research for tungsten nitride (WN) is not carried out enough. However, it is expected that as WN has a wide variety of composition range of β-W_2N expected to have good characteristics as a diffusion barrier, it is thought that the process windows would be wide, and as there is a advantage of having a precursor which is gaseous WF_6, it is favorable to

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mass production. However, referring to the results of research to now, it has not superior characteristics than the conventional diffusion layers. Particularly, the reports to characteristics of the diffusion barrier against copper are few.

Also, the research is being performed so as to form an amorphous diffusion layer to remove completely the grain boundary which acts as a path to diffuse easily for copper. That is, the research for replacing polycrystalline layer with amorphous layer by adding silicon or boron to Ti-N, Ta-N, or W-N group. however, though there is ever deposited a diffusion barrier having good characteristics by PVD, the research for CVD is hardly carried out.

FIGS. 1 to 6 illustrate an embodiment of a method for forming copper interconnect structure according to the present invention. Referring to FIG. 1, there is provided a portion of a semiconductor device, which includes a substrate 10 and a dielectric film 20 overlying the substrate 10. On the substrate 10, several components may be formed, such as metal oxide semiconductor (MOS), bipolar junction transistor (BJT) , resistor, and the like. Such components are formed before the step shown in FIG. 1.

Meanwhile, the semiconductor device may employ multi-layer wiring structure. In such a case, the substrate 10 may include a metal interconnect layer connecting the components electrically. A dielectric film 20 may be SiO_2, SiN_4, or doped glass. The dielectric film 20 can be formed using CVD, plasma enhanced chemical vapor deposition (PECVD), and the like. In a preferred embodiment of the present invention, the SiO_2 is deposited by CVD to form the dielectric film 20.

Referring to FIG. 2, a via pattern 22 is formed on the substrate 10. The via pattern 22 is formed by reactive ion etching using a mask defining its boundary. In a contact hole with which metal wire contacts the components on the substrate 10 or the underlying metal wire, the via

pattern 22 is formed to extend to the substrate 10 through the dielectric film 20.

As shown in FIG. 3, the TiN layer 32 is formed to overlie the dielectric film 20 on which the via pattern 22 is formed. In a preferred embodiment, the TiN layer is formed to the thickness of less than 200 anstroms (Å). Afterwards, an aluminum layer 34 is formed on the TiN layer 32 by CVD as shown in FIG. 4. In a preferred embodiment, the aluminum layer is deposited to the thickness of about 5 to 20 nanometers (nm). The composite structure of TiN layer 32 and aluminum layer 34 functions as a diffusion barrier. The TiN layer 32 also acts as a seed layer (promoter layer) for CVD-Al and as a etch-stop layer for CMP process.

Referring to FIG. 5, a copper layer 40 is deposited so that the via pattern 22 is filled sufficiently. The deposition of the copper layer 40 is carried out by PVD, electroplating or metal organic chemical vapor deposition (MOCVD). Following the deposition of the copper layer 40, the semiconductor device is planarized as shown in FIG. 6. In a preferred embodiment, the planarization process is performed with chemical mechanical polishing (CMP) by non-selectively removing the copper layer 40, the aluminum layer 34, and the TiN layer 32 . Meanwhile, in an alternative embodiment, the planarization may be performed with non-selective plasma etching process. Upon completing the planarization, the copper pattern 50 is exposed on the dielectric film 20, and the diffusion barrier 30 including the TiN layer 32 and aluminum layer 34 is inserted between the dielectric film 20 and the copper pattern 50.

FIGS. 7 to 8 shows experimental data in accordance with the copper interconnect structure of the present invention. In the experiments, a TiN layer is deposited to the thickness of 200 angstroms by pyrolytic deposition using the single precursor of the TDMAT on 8 inch silicon wafer. After the sample is cut to the size of 1x1 inches, aluminum and copper is deposited

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sequentially using direct current (DC) magnetron sputter and annealed at a pressure of below $5x10^{-6}$ torr in a vacuum ambient. The annealing is carried our for about an hour and the annealing temperatures are differentiated with an interval of 50°C at the range of 500 to 700°C. The sheet resistance of the sample is measured with a four-point probe after the annealing is completed . FIG. 7 shows the measured sheet resistance of the samples depending on the thickness of aluminum and the annealing temperature. As shown in FIG. 7, the sample deposted with aluminum to the thickness of above 10 nanometer prevents the diffusion more effectively than the sample A which has not the aluminum layer.

Next, to evaluate the breakdown temperature of the diffusion barrier, secco etching is carried out to the surface of the silicon, after removing the copper layer , aluminum layer, and the TiN layer using a chemical solution. FIGS. 8A to 8D are photographs observed by use of scanning electron microscopy showing etch pits of silicon surface exposed after completion of the etching . FIGS. 8A to 8D correspond to the four kinds of samples A, B, C, and D, respectively, all of which are annealed at a temperature of 650°C. As shown in the drawings, as the thickness of the aluminum layer increases, the density and the size of etch pit decreases abruptly.

Referring to the results of the measurement regarding the breakdown temperature, the sample without the aluminum layer is failed after the annealing for an hour at a temperature of 500°C in a vacuum ambient, whereas the sample deposited with aluminum to the thickness of above 10 nanometer is not failed ,even after the annealing for an hour at a temperature of 700°C in a same ambient. This strongly demonstrates that the combination of TiN and aluminum shows a superior diffusion barrier property against copper diffusion.

Meanwhile, although the invention has been descried and illustrated with reference to specific illustrative embodiments thereof, it is not intended

that the invention be limited to those illustrative embodiments. Those skilled in the art will appreciate that many obvious modifications can be made without departing from the spirit or essential charcteristics of the present invention. For example, metal other than aluminum, such as zirconium (Zr), titanium (Ti), and chrome (Cr) may be employed for the intermediate metal layer alternatively. Also, though the intermediate metal layer is formed with a single layer in the preferred embodiments, it may be formed with multi-layered structure. Furthermore, the intermediate metal layer may be formed by a process such as PVD, electrode plating, electrodeless plating, wet chemical contamination, and atomic layer deposition (ALD) instead of chemical vapor deposition. Even though titanium nitride (TiN) is illustratively used for the diffusion barrier in the preferred embodiments, tantalum nitride (TaN) or tunsten nitride (WN) may be used for the barrier alternatively. Further, the diffusion barrier may be deposited by chemical deposition, also.

In the description above, the method for forming the copper interconnect has been illustrated in terms of the interconnect extending on the dielectric film without mentioning a contact hole. Actually, however, there may be formed the contact hole with which metal wire contacts the components on the substrate or the underlying metal wire.

In such a contact hole, a diffusion barrier is deposited on the substrate at the bottom of the contact hole on the underlying the metal wire, and an intermediate metal layer is deposited onto the diffusion barrier. A copper layer is then deposited onto the intermediate metal layer. Meanwhile, in an alternative embodiment, it may be possible to form an ohmic contact in the contact hole depositing the intermediate metal layer without the copper layer and employing the copper interconnect structure only in the field region.

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What is claimed is:

1. A method of fabricating semiconductor device employing copper interconnect strcture comprising the steps of:

forming a dielectric film overlying a semiconductor substrate;

forming a diffusion barrier overlying the dielectric film;

forming an intermediate metal layer overlying the diffusion barrier; and

forming a copper layer overlying the intermediate metal layer.

2. The method as claimed in claim 1, further comprising the step of : annealing the semiconductor device having the copper layer so that an oxide compound of an intermediate metal material forming the intermediate metal layer stuff grain boundaries of the diffusion barrier.

3. The method as claimed in claim 1, wherein the intermediate metal layer is formed by use of one selected from the group consisting of aluminum (Al), zirconium (Zr), titanium (Ti), chrome (Cr), and a combination thereof.

4. The method as claimed in claim 3, wherein the intermediate metal layer consists of multiple layers.

5. The method as claimed in claim 3, wherein the intermediate metal layer is formed with a process selected from the group consisting of PVD, electrode plating, electrodeless plating, wet chemical contamination, and atomic layer deposition.

6. The method as claimed in claim 3, wherein the diffusion barrier is formed by use of one selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), and tungsten nitride (WN).

7. Method of fabricating semiconductor device employing copper interconnect structure comprising the steps of:

forming a dielectric film overlying a semiconductor substrate;

forming a via pattern overlying the dielectric film;

forming a diffusion barrier overlying the via pattern using one selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), and tungsten nitride (WN);

forming an intermediate metal layer overlying the diffusion barrier using one selected from the group consisting of aluminum (Al), zirconium (Zr), titanium (Ti), chrome (Cr), and a combination thereof;

forming a copper layer overlying the intermediate metal layer; and

annealing the semiconductor device having the copper layer so that an oxide compound of an intermediate metal material forming the intermediate metal layer stuff grain boundaries of the diffusion barrier.

8. Method of fabricating semiconductor device employing copper interconnect structure comprising the steps of:

forming a first copper layer overlying a semiconductor substrate;

forming a dielectric film overlying the first copper layer;

forming a contact hole exposing the first copper layer by etching the dielectric film;

forming a diffusion barrier overlying the dielectric film and the contact hole using one selected from the group consisting of titanium nitride (TiN), tantalum nitride (TaN), and tungsten nitride (WN);

forming an intermediate metal layer overlying the diffusion barrier

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using the one selected from the group consisting of aluminum (Al), zirconium (Zr), titanium (Ti), chrome (Cr), and a combination thereof;

forming a second copper layer overlying the intermediate metal layer; and

annealing the semiconductor device having the copper layer so that an oxide compound of an intermediate metal material forming the intermediate metal layer stuff grain boundaries of the diffusion barrier.

FIG. 1

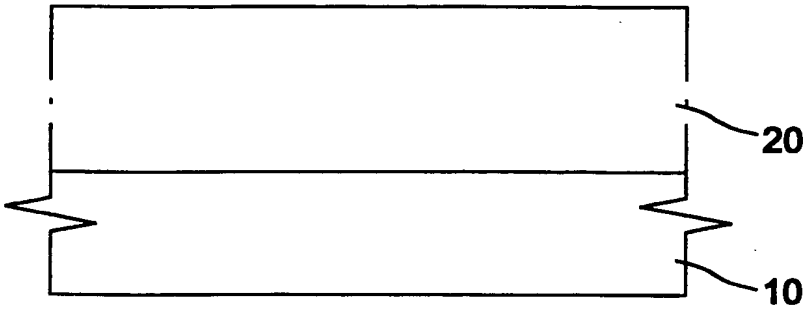

FIG. 2

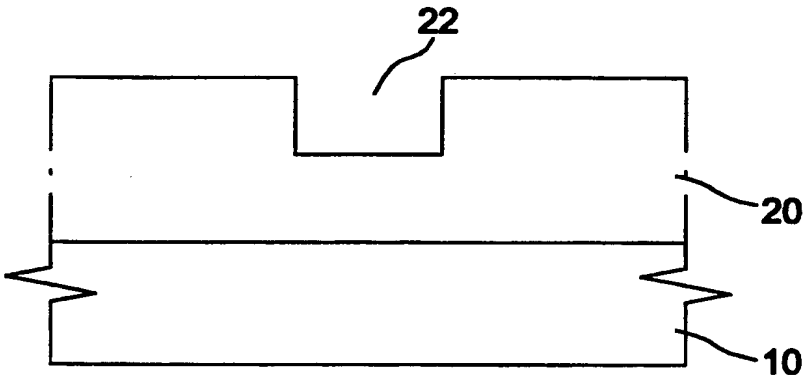

FIG. 3

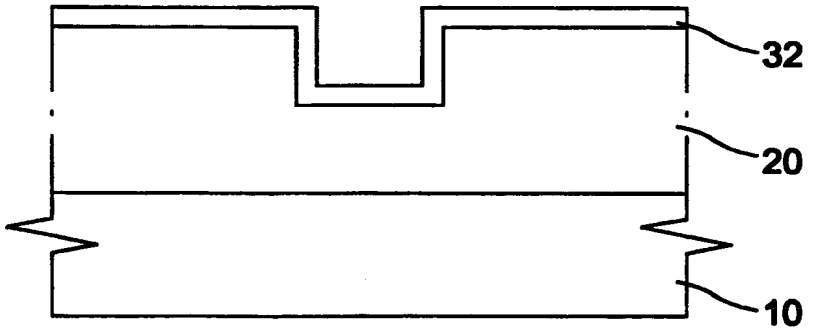

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FIG. 4

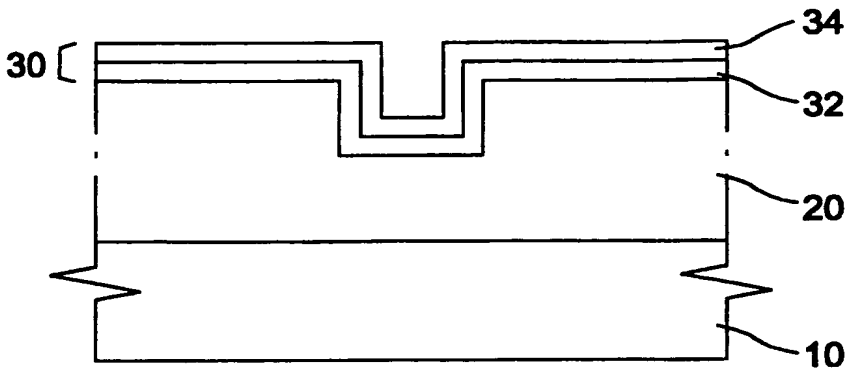


FIG. 5

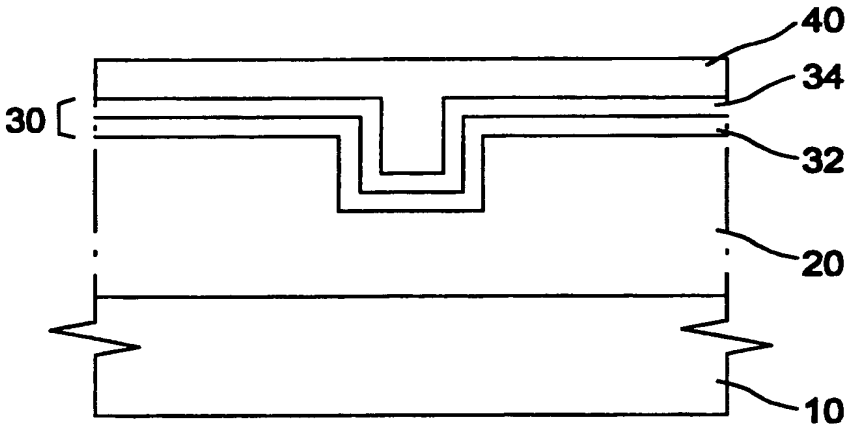


FIG. 6

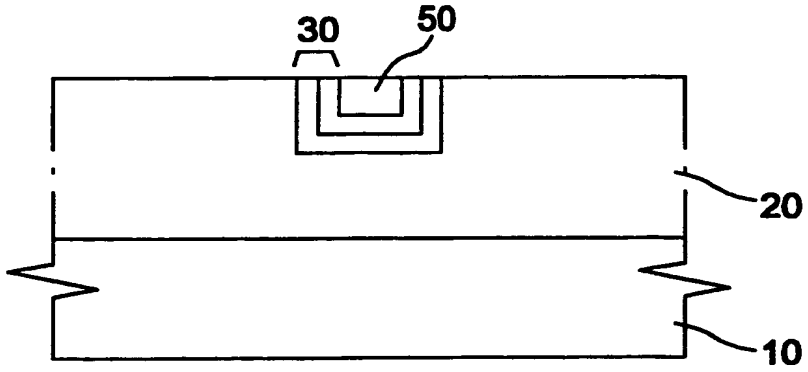
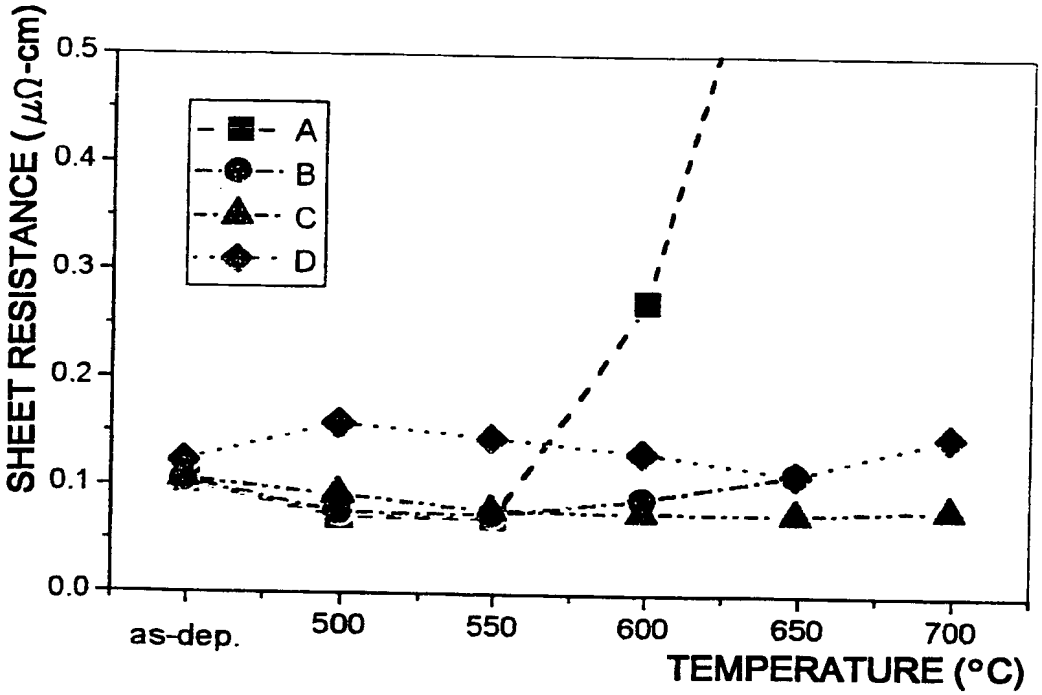


FIG. 7



SAMPLE A : Cu(300nm) / TiN(20nm) / Si
SAMPLE B : Cu(300nm) / Al (5nm) / TiN(20nm) / Si
SAMPLE C : Cu(300nm) / Al (10nm) / TiN(20nm) / Si
SAMPLE D : Cu(300nm) / Al (20nm) / TiN(20nm) / Si

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FIG. 8A

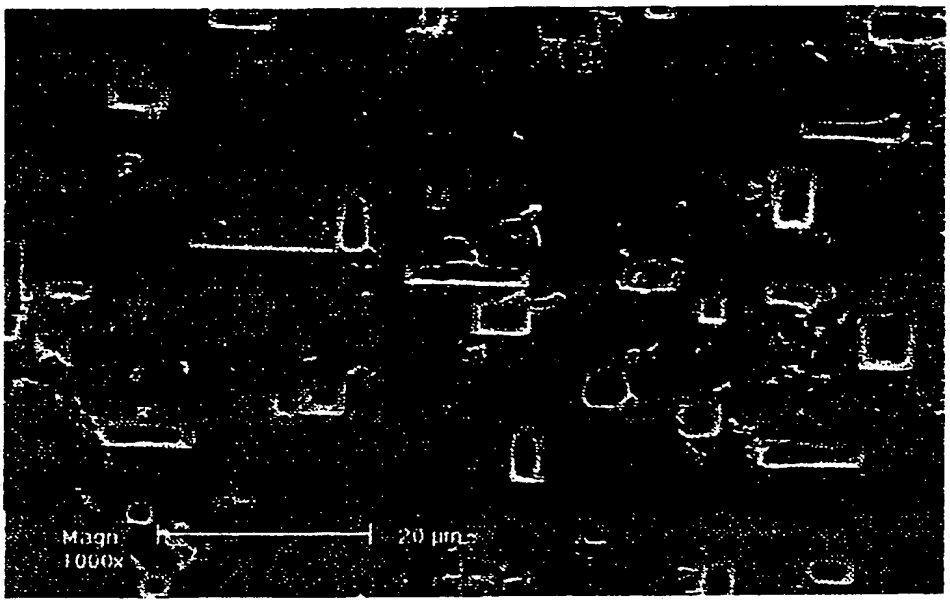


FIG. 8B

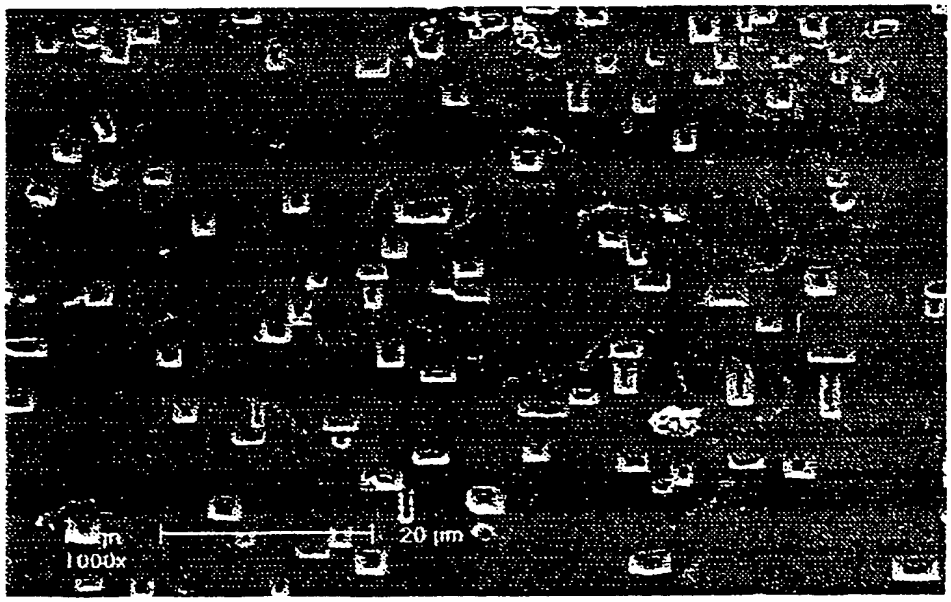


FIG. 8C

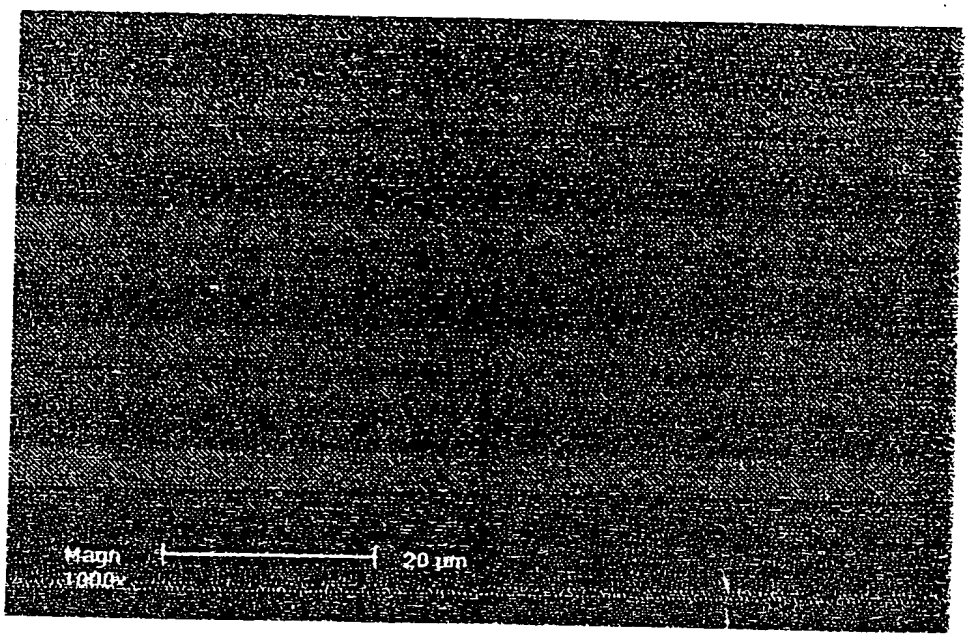
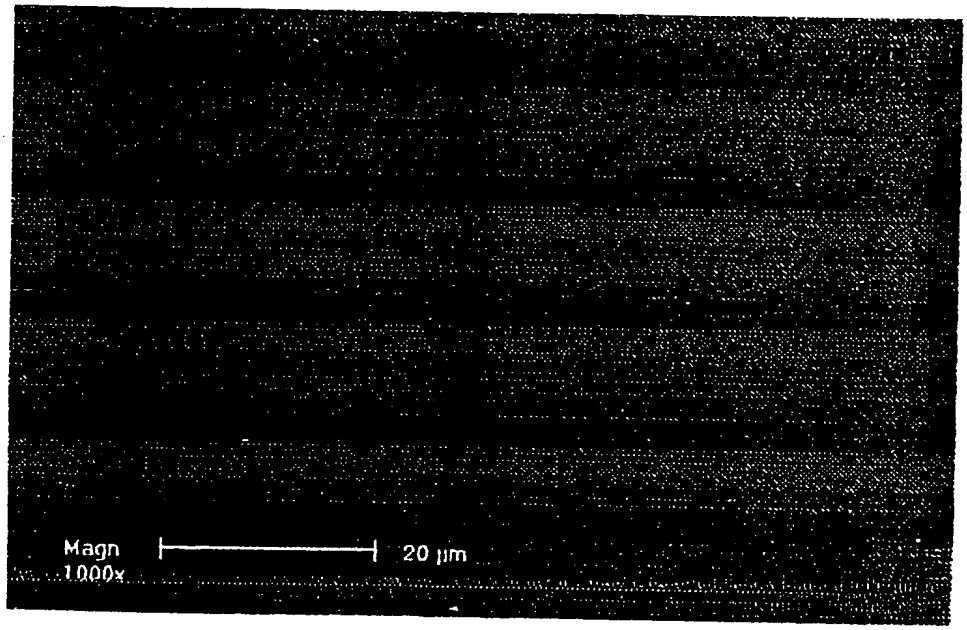


FIG. 8D



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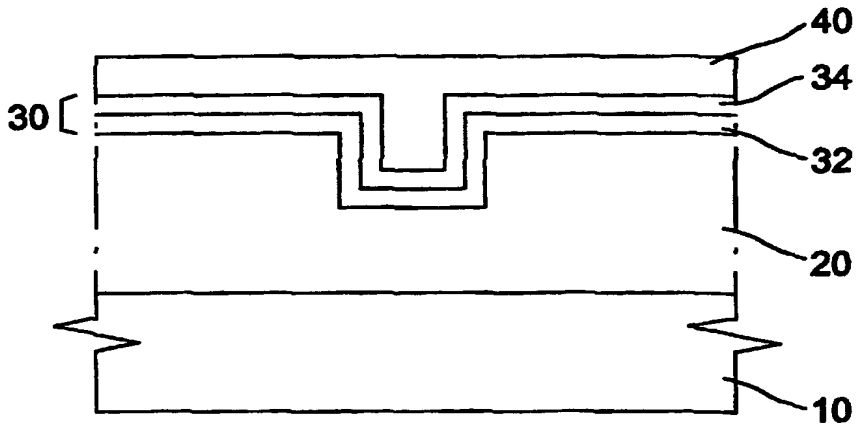

(57) Abstract: The present invention provides a method of forming interconnect structure in a process for fabricating semiconductor device, which enables high-reliability copper interconnect. The present invention uses the structure comprised of TiN layer (32) and intermediate aluminum layer (34) as a diffusion barrier. A copper layer (40) is deposited on the aluminum layer (34), after aluminum layer (34) is deposited on the TiN layer (32). At this time, with the aluminum layer (34) being made to the minimum thickness, metallization is formed substantially with the copper.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00847

CLASSIFICATION OF SUBJECT MATTER

IPC[7]: H 01 L 23/52, 23/535, 23/532, 21/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7]: H 01 L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, PAJ-Database

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5592024 A (AOYAMA) 7 January 1997 (07.01.97) abstract; description column 2, lines 11-20; column 9, lines 55-61; column 10, lines 1-2; claims 1-5.	1-3,5,6 7,8
X Y	US 5674787 A (ZHAO) 7 October 1997 (07.10.97) abstract; description column 8, lines 50-65; claims 1-32.	1 7,8
X A	US 5595937 A (MIKAGI) 21 July 1997 (21.07.97) abstract.	1 2-8
A	US 5275973 A (GELATOS) 4 January 1994 (04.01.94) abstract. ----	1-8

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
„A" document defining the general state of the art which is not considered to be of particular relevance
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„P" document published prior to the international filing date but later than the priority date claimed

„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 April 2000 (14.04.2000)	31 July 2000 (31.07.2000)
Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	Authorized officer Mayer Thomas Telephone No. 1/53424/452

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR 99/00847

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US A 5592024	07-01-1997	JP A2 7307338	21-11-1995
		KR B1 169283	01-02-1999
US A 5674787	07-10-1997	none	
US A 5595937	21-01-1997	JP A2 8288389	01-11-1996
		JP B2 2728025	18-03-1998
US A 5275973	04-01-1994	none	

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